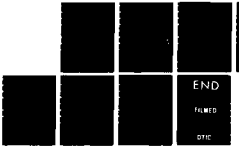
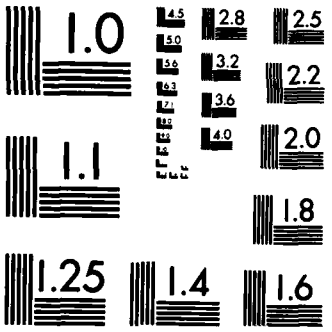
AD-A157 343 SURFACE AND INTERFACIAL PROPERTIES OF GA047IN053AS ALLOYS(U) CALIFORNIA UNIV SAN DIEGO LA JOLLA DEPT OF ELECTRICAL ENGINEE... H H WEIDER 15 JUL 85 1/1

UNCLASSIFIED N00019-84-C-0169 F/G 11/6 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Surface and Interfacial Properties of $Ga_{0.47}In_{0.53}As$ Alloys		5. TYPE OF REPORT & PERIOD COVERED Final Report April 1, '84 to March 31,'85 6. PERFORMING ORG. REPORT NUMBER
AUTHOR(s) H. H. Wieder		8. CONTRACT OR GRANT NUMBER(s) N00019-84-C-0169
PERFORMING ORGANIZATION NAME AND ADDRESS University of California, San Diego Electrical Engineering & Computer Sciences Dept. C-014, La Jolla, CA 92093		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
CONTROLLING OFFICE NAME AND ADDRESS Naval Air Systems Command Washington, DC 20361, Code AIR 33R		12. REPORT DATE July 15th, 1985 13. NUMBER OF PAGES
MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Office of Naval Research, Resident Representative La Jolla (Q-043) University of Cal., San Diego La Jolla, CA 92093		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Gallium Indium Arsenide; Semiconductor Surface and Interfacial Properties; Dielectric-Compound Semiconductor Interfaces.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

See page 1.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE
S/N 0102-LF-014-6601

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

Final Report

April 1st, 1984 to May 31, 1985

Surface and Interfacial Properties of $Ga_{0.47}In_{0.53}As$ Alloys

Contract: N00019-84-C-0169

Naval Air Systems Command, Code AIR-33R

Principal Investigator: H. H. Wieder

Department of Electrical Engineering and Computer Sciences

University of California, San Diego

La Jolla, California 92093

A-1

Abstract

A modified Varian GenII. molecular beam epitaxial deposition system was installed and preliminary performance tests have indicated its suitability for growing binary and ternary III-V alloy semiconducting layers. Gallium arsenide layers grown with this MBE system have electrical properties which compare well with those of the best layers grown elsewhere. One 50 layer GaAs/$Ga_xAl_{1-x}As$ (160 Å per layer thick) superlattice was used to test the usefulness of the MBE system for the synthesis of conventional heterojunctions and superlattices. Preliminary results have been obtained with $Ga_{0.47}In_{0.53}As$ epitaxial layers whose lattice constant matches exactly that of their InP substrates. Work is underway on the synthesis of the ternary alloy layers and heterojunctions whose lattice constants match that of InP.

Introduction

Semiconducting $Ga_{0.47}In_{0.53}As$ layers whose lattice constants match that of semi-insulating InP are, potentially, useful for discrete and integrated circuit microwave transistors and opto-electronic sensors compatible with the low loss, low dispersion spectral window of optical fibers. Their implementation requires evaluation, modelling and interpretation of the surface and interfacial properties of this ternary semiconducting compound in terms of fundamental physical parameters.

The projected application of $Ga_{0.47}In_{0.53}As$ keep on expanding. They now include field effect transistors with insulated gates, junction gates and, at least potentially, modulation-doped transistors similar to those based on two-dimensional electron gas phenomena in GaAs-based heterostructures made by molecular beam epitaxial techniques. In addition to the electro-optic detector applications for 1.3 to 5.3 μm (in wavelength) planar photoconductive detectors based on the compensated semi-insulating material described in our invention disclosure were developed at the Lincoln Laboratory, Lexington, Ma. Quantum efficiencies of the order od 40% in the 1 to 1.6 μm spectral range and speeds of 50 to 90ps were obtained with these devices. MBE techniques are particularly well suited for making single and multiple heterojunctions grown on semi-insulating or conducting substrates with controlled doping concentrations and interfaces. Such heterojunctions are used at this time for solid state lasers, photodetectors and research is underway to apply them for bipolar high-speed transistors. The theoretical aspects of heterojunction interfaces are to a large extent not known or understood; most of recent experimental verification of theoretical predictions have concentrated on the GaAs-GaAlAs heterojunction system because a great deal is known about the synthesis, interfacial properties and impurity

doping with both donors and acceptors of this system. However, the availability of the two ternary alloys: $In_{0.52}Al_{0.48}As$ with a fundamental room temperature bandgap of 1.47 eV and $Ga_{0.47}In_{0.53}As$ with a bandgap of 0.765 eV lattice matched to InP with a bandgap of 1.34 eV provide a greater range of heterojunction choices. The relations between the fundamental bandgaps of Si, Ge and III-V compound binary and ternary alloys and their corresponding lattice constants are illustrated in Fig. 1.

Many of the proposed heterojunction device applications require a good understanding of band offsets. For example: a heterostructure equivalent of a photomultiplier such as proposed by Williams, Capasso and Tsang [IEEE Electron Dev. Lett. 3, 71 (1982)] requires a highly assymetric band lineup with a conduction band offset which is larger than the fundamental bandgap of the narrower bandgap semiconductor and a valence band offset which is as small as possible. This requires a reasonably quantitative prediction theory of band lineups. Neither experimental data, nor sufficient empirical information is, as yet available to provide full confirmation of proposed theoretical concepts. Although substantial progress is being made no completely reliable theory, starting from first order assumptions is, as yet, available. The choice of a particular semiconductor pair for heterojunctions is also dependent on their compatibility with other desiderata for electronic device applications.

Experimental evidence is accumulating that the band offsets are technological process-dependent; that to some extent, at least, they depend on the heterojunction growth procedures and crystallographic orientations. It appears, furthermore, that in the case of multiple heterojunctions those grown initially are different from those grown subsequently.

The overwhelming majority of all semiconductors employed for

heterojunctions are those based on the $Al_xGa_{1-x}As$-GaAs system in which very good lattice matching is obtained over the entire compositional range.

The $Ga_{.47}In_{.53}As/Al_{.48}In_{.52}As$ material system is analogous to $GaAs/Al_xGa_{1-x}As$ in that both systems consist of a lower bandgap, high electron mobility, material which is lattice matched to a higher bandgap material.

Field effect transistors made from modulation doped $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ lattice matched to InP are likely to have superior performance at high frequencies and the microwave range compared to conventional devices. Mobility of electrons in $Ga_{0.47}In_{0.53}As$ at all doping levels is 50% higher than that in GaAs. Electron saturation velocity in doped MESFET channels has been found to be lat least 25% higher than that of GaAs. Modulation doped AlInAs/GaInAs heterojunction MODFET's with ~ 1 micron source-drain spacing might have a more than 2×10^7cm/s mean electron velocity at 300°K, compared with the $1.6\text{-}1.8 \times 10^7$cm/s for AlGaAs/GaAs MODFETS.

Electrons in $Ga_{0.47}In_{0.53}As$ can reach a higher energy (.42-.55 eV) before transferring to the heavy mass conduction band minima compared with GaAs (.35-.36 eV). The exact values relevant to the upper conduction band minima in the GaInAs have not been determined as yet. The electron peak group velocity limit in $Ga_{0.47}In_{0.53}As$ is ~ 10^8cm/s. The heterojuction conduction band offset between AlInAs and GaInAs is .52-.66 eV. Thus electrons might reach their peak group velocity, or even a limiting upper conduction band valley velocity without having enough energy to pass across the heterojunction interface. In the case of the AlGaAs/GaAs heterojunction the upper valley energy of .35-.36 eV in the GaAs does not limit the electrons from reaching the less than .20 eV heterojuction barrier energy. In consequence electrons in GaAs MODFET experience real space transfer into the AlGaAs, where their

velocity is reduced sharply.

Progress

The major effort underway at UCSD during the past year has been concerned with the installation and the initial checkout of the molecular beam epitaxial deposition system.

A Grant of $257,000 provided by the U.S. Air Force Office of Scientific Research under the Department of Defense - University Research Instrumentation Program (FY 1983) to the University of California, San Diego in La Jolla, CA, 92093, was used as partial support for the purchase of a Molecular Beam Epitaxial (MBE) Deposition Machine. Additional funds were provided by the National Science Foundation, by UCSD intramural contributions, by the Powell (private) foundation and a major equipment donation from Varian Associates for a total of $471,000.

The MBE machine purchased, installed and presently in operation is a modified Varian Associates Gen.II Machine without the low energy electron diffraction and without the Auger surface spectrometer. The system is superior to the older model Varian 360 but inferior to the Gen.II model which is, however, more expensive by an estimated $300,000.

The machine was delivered in June 1984. However, some additional components, primarily Knudsen effusion cells and a Quadrupole Mass Spectrometer, donated by Varian Associates were not delivered until July 1984. From August through October initial checkout procedures indicated minor defects: an out of round transfer rod, a broken heater filament in the substrate holder and some defective linkage in the specimen loader. These were easily repaired and from October 1984 through December 1984 we have gone through the initial checkout procedures for growing epitaxial layers. During that period, twelve gallium arsenide single crystal layers were grown on semi-insulating gallium

arsenide substrates in the thickness range between 2.5 micrometers to 0.05 micrometers of excellent morphological characteristics.

These undoped layers were found to be p-type with a typical hole density of $p = 2.49 \times 10^{14}/cm^3$ and a mobility $w_p = 334\ cm^2/V\text{-sec}$. Similar results were obtained by other researchers in the U.S., the U.K. and Japan; the p-doping is attributed to carbon monoxide contamination inherent in the MBE growth chamber. Compensating these impurities was accomplished by doping the layers during their growth with silicon. We have produced such lightly doped n-type GaAs layers in the MBE chamber with an electron concentration, $n = 1.88 \times 10^{15}/cm^3$ and mobility, $\mu_n = 6.44 \times 10^3\ cm^2V\text{-sec}$. These values are in excellent agreement with theoretical expectations and with the experimental data of others using similar MBE machines.

From January 1985 through May 1985 we were engaged in further qualification tests of the MBE machine intended to demonstrate its usefulness to produce ternary alloys, heterojunctions and superlattices. We started with the ternary alloy $Ga_xAl_{1-x}As$ because considerable, albeit empirical, information is available on the parametric controls required for its synthesis by MBE. The growth of ternary alloys is more complicated than that of binary alloys. After a few false starts we managed to grow morphologically high quality $Ga_xAl_{1-x}As$ layers by choosing optimum molecular beam flux ratios of the constituents with a relatively moderate substrate temperature of 680^0C.

We have also grown one $GaAs/Ga_xAl_{1-x}As$ superlattice structure made up of 50 alternating GaAs and $Ga_xAl_{1-x}As$ layers each 160 Å in thickness. No electrical or optical characterization of these layers has been made as yet. This awaits completion of Hall effect apparatus and the construction of a photoluminescence spectrometer presently underway at UCSD.

During this time period we also encountered a severe problem with the MBE system which, fortunately, has since been remedied. We discovered the presence of water vapor in the MBE chamber and traced its origin to a hairline crack which had developed in the water-cooling jacket of the titanium ball sublimation pump. Fortunately, this was still under warranty; we received an immediate replacement from Varian Associates and since its installations we obtain, in a routine manner vacuum levels of the order of 10^{-10}.

Since May 1985 we have been growing ternary alloy $Ga_xIn_{1-x}As$ epitaxial layers on n-doped and on semi-insulating InP. We are trying to achieve the right conditions for producing an exact lattice match between this ternary alloy and its InP substrate, prevent outdiffusion of Fe from the SI substrate, obtain an abrupt interface between the epilayer and its substrate and obtain the maximum electron mobility consistent with doping concentration.

Thus far we have grown 0.50 μm and 0.25 μm thick $Ga_xIn_{1-x}As$ layers with both, x larger than and smaller than x = 0.47, in order to determine the precise effusion cell temperatures and flux ratios for synthesizing the exact conditions for the lattice matched composition. The unmatched epilayers contain segmented misfit dislocations clearly visible using Normarski interference microscopy. Well matched epilayers of $Ga_{0.47}In_{0.53}As$ have now been grown. They contain a few isolated morphological defects which appear to be dislocation clusters.

We propose to continue to refine the MBE growth process in order to eliminate the above described minor defects and then to proceed with the optical, electrical and galvanomagnetic charactization of the $Ga_{0.47}In_{0.53}As$ epilayers. Thereafter, we propose to perform the same investigation on the lattice matched $In_{0.52}Al_{0.48}As$ to their semi-insulating InP substrates.

Publications and Patents

During the period of this contract the following publications and relevant patents have appeared:

1. Interface Constraints on MESFET and MISFET Architectures, by H. H. Wieder, Chapter V in VLSI Electronics: Microstructure Science, Surface and Interface Effects in VLSI, edited by Norman M. Einspruch; Monograph, Academic Press (1985) pp. 167-235.

2. U. S. Patent No. 4, 468, 851, Process for making heterojunction source-drain insulated gate field effect transistors utilizing diffusion to form the lattice; H. H. Wieder and A. R. Clawson. Date of patent: September 4, 1984.

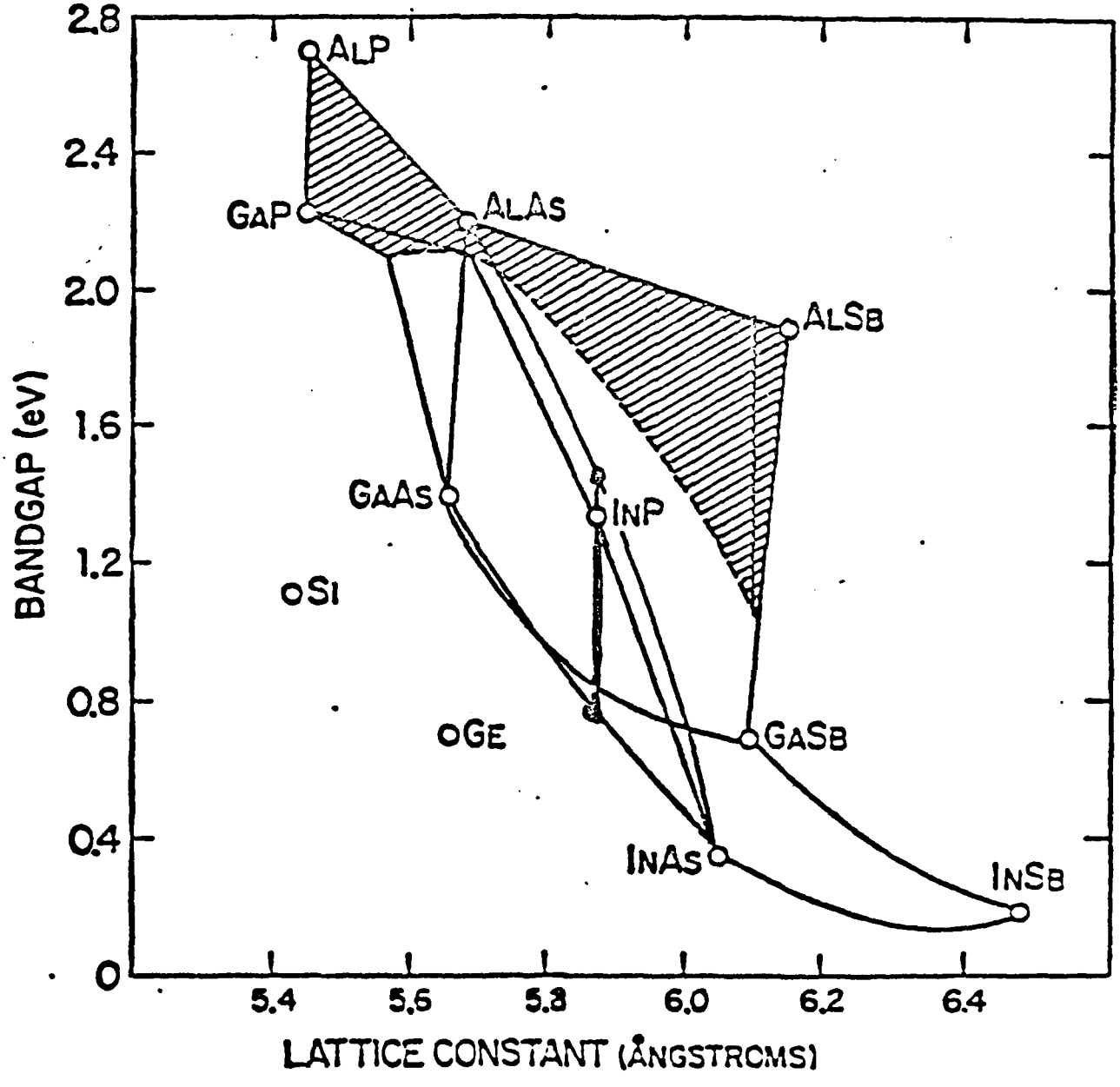


Figure 1 Energy bandgap versus lattice constant for some III-V compounds and their corresponding alloy systems.

United States Patent [19]

Wieder et al.

[11] **Patent Number: 4,468,851**

[45] **Date of Patent: Sep. 4, 1984**

[54] **PROCESS FOR MAKING A HETEROJUNCTION SOURCE-DRAIN INSULATED GATE FIELD-EFFECT TRANSISTORS UTILIZING DIFFUSION TO FORM THE LATTICE**

[75] Inventors: **Herman H. Wieder; Arthur R. Clawson**, both of San Diego, Calif.

[73] Assignee: **The United States of America as represented by the Secretary of the Navy**, Washington, D.C.

[21] Appl. No.: **330,281**

[22] Filed: **Dec. 14, 1981**

[51] **Int. Cl.**³ **H01L 21/223**; H01L 21/20

[52] **U.S. Cl.** ..... **29/571**; 29/576 E; 29/578; 29/580; 29/591; 148/175; 148/187; 156/648; 357/22; 357/23; 357/16

[58] **Field of Search** ..... 29/571, 576 E, 578, 29/580, 591; 148/175, 187; 156/648, 655, 662; 357/22 P, 23 NS, 16, 61

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,351,828	11/1967	Beale et al.	357/16
3,982,261	9/1976	Antypas	148/175 X
4,075,651	2/1978	James	357/61 X
4,160,261	7/1979	Casey et al.	357/23 NS
4,186,407	1/1980	Delagebeaudeuf	357/13
4,350,993	9/1982	Wieder	357/22 X

OTHER PUBLICATIONS

Wieder et al., "Inversion-Mode Insulated Gate $Ga_{0.47}In_{0.53}As$-", IEEE Electron Device Letters, vol. EDL-2, No. 3, 1981, pp. 73-74.

Leheny et al., "Am $In_{0.53}Ga_{0.47}As$ Junction Field-Effect Transistors", IEEE Electron Device Letters, vol. EDL-1, No. 6, Jun. 1980, pp. 110-111.

Terman, L. M., "MOSFET Structures Using Selective Epitaxial Growth", IBM Tech. Discl. Bull., vol. 13, No. 11, Apr. 1971, pp. 3279-3280.

Fukuta et al., "Power GaAs MESFET-", IEEE Trans. on Microwave Theory & Tech., vol. MTT-24, NO. 6, Jun. 1976, pp. 312-317.

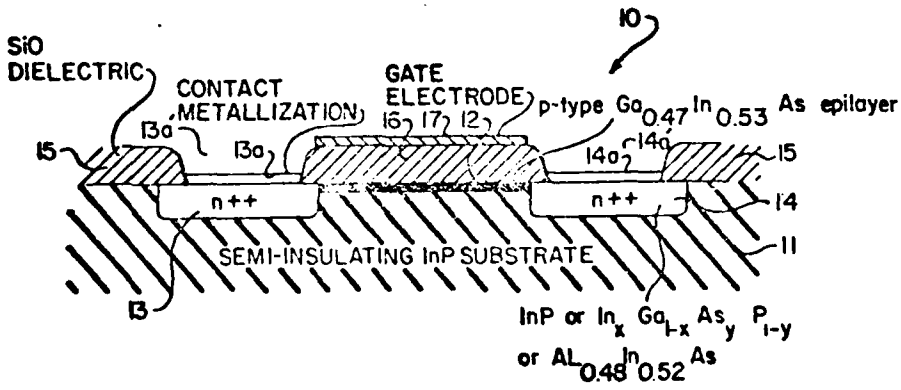
Primary Examiner—William. G. Saba

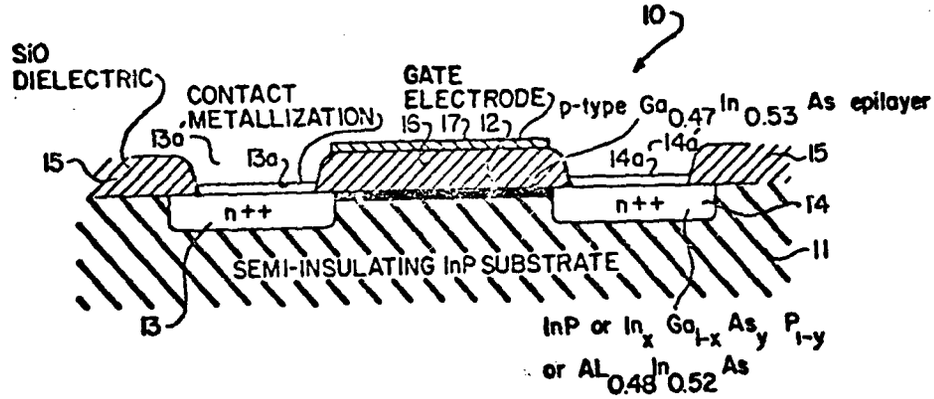
Attorney, Agent, or Firm—Robert F. Beers; Ervin F. Johnston; Thomas Glenn Keough

[57] **ABSTRACT**

An apparatus for and a method of making heterojunction source-drain insulated gate field-effect transistors in order to obtain higher gain-bandwidth products at microwave frequencies. A semi-insulating InP semiconductor substrate is provided with a ternary alloy layer of p-type $Ga_{0.47}In_{0.53}As$, or optionally, an acceptor-doped p-type bulk of $Ga_{0.47}In_{0.53}As$ can be substituted. Troughs are shaped in the substrate and layer for receiving a material lattice-matched to the n^+ p-type $Ga_{0.47}In_{0.53}As$ to perform as the source and drain contacts, n^+ doped InP might be a suitable material. An optional method for forming the contacts calls for directing a stream of phosphine and hydrogen onto source and drain contact windows contacting the $Ga_{0.47}In_{0.53}As$ which is heated to 750° C. for about 15 minutes. This creates graded heterojunction source and drain contacts having a lattice-matching variable composition.

3 Claims, 1 Drawing Figure




10
SiO
DIELECTRIC
CONTACT
METALLIZATION
GATE
ELECTRODE
16 17 12
p-type Ga0.47 In0.53 As epilayer
15
13a
13a
14a
14a
15
n++
n++
14
11
SEMI-INSULATING InP SUBSTRATE
13
InP or Inx Ga1-x Asy P1-y
or AL0.48 In0.52 As

PROCESS FOR MAKING A HETEROJUNCTION SOURCE-DRAIN INSULATED GATE FIELD-EFFECT TRANSISTORS UTILIZING DIFFUSION TO FORM THE LATTICE

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to an application filed Dec. 14, 1981 in the U.S. Patent and Trademark Office, Ser. No. 330,283, by Herman H. Wieder entitled "Inversion-Mode Insulated Gate $Ga_{0.47}In_{0.53}As$ Field-Effect Transistor".

BACKGROUND OF THE INVENTION

This invention relates to the field of FETs having improved higher frequencies and larger gain-bandwidth capabilities. More particularly inversion mode operation between heterojunction contacts through a p-type ternary alloy epilayer permits faster electron transit.

The only inversion mode field-effect transistors, other than silicon devices, are those employing indium phosphide or such as described by H. H. Wieder et al in IEEE Electron Device Letters, Vol. EDL-2, page 73 (1981) which are the basis of this invention.

The above cited related invention of H. H. Wieder represents still another advance in the state-of-the-art for improving the capability of the field-effect transistor. It discloses the use of p-type $Ga_{0.47}In_{0.53}As$ in an epilayer under an insulated gate electrode and touching the source and drain contacts to help assure improved operational capabilities.

Although U.S. Pat. No. 3,982,261 to George A. Antypas discloses a quarternary alloy layer lattice-matched to an InP substrate, his application has been used for improving the responses of photocathodes and lasers. The energy bandgap differences are utilized to enhance the infrared sensitivity and to provide means for varying the operating wavelengths of a solid state laser. Antypas does not appreciate the favorable properties of the disclosed materials for use in a heterojunction field-effect transistor.

The disclosure of the U.S. Pat. No. 4,186,407 concerns the use of $Ga_{0.47}In_{0.53}As$ to fabricate avalanche diodes intended to function as oscillators. The purpose and intent of this patent also is distinct from that of using heterojunction source and drain contacts and an insulated gate electrode for assuring improved operational characteristics of a field-effect transistor.

Thus, there is a continuing need in the state-of-the-art for a heterojunction source-drain insulated gate field-effect transistor in which lattice-matching materials are advantageously employed for the source and drain contacts to assure improved operational capabilities.

SUMMARY OF THE INVENTION

The present invention is directed to providing a method of making an inversion mode metal-insulator-semiconductor field-effect transistor having heterojunction source and drain contact junctions. First, there is the providing of a semi-insulating semiconductor substrate and a growing of a ternary alloy layer of p-type $Ga_{0.47}In_{0.53}As$ epitaxially on a portion of the semi-insulating semiconductor substrate. Next, there is the coating of the exposed semi-insulating semiconductor substrate and the ternary alloy layer with a dielectric. Opening source and drain contact windows through the dielectric coating that are in contact with the ternary al. y layer permits the depositing of a material lattice-matched to the p-type ternary alloy layer through the source and drain contact windows to form the heterojunction source and drain contacts. Superposing a metal gate electrode on a dielectric layer covering the ternary alloy layer in a region lying between the heterojunction source and drain contacts allows potential variations to produce an inversion mode control of the electron flow between the heterojunction source and drain contacts.

The prime object of the invention is to provide an improved method of fabricating a field-effect transistor.

Still another object is to provide a method for fabricating a heterojunction field-effect transistor.

Still another object is to provide a method for fabricating a heterojunction field-effect transistor employing an epitaxial grown p-type $Ga_{0.47}In_{0.53}As$ layer on a semi-insulating semiconductor substrate.

A further object is to provide a field-effect transistor having negligibly small currents due to the inclusion of heterojunction source and drain contacts.

Another object of the invention is to provide a method for fabricating a heterojunction field-effect transistor having the possibility for optical excitation of either heterojunction and optically-induced modulation coupled to the transistor action of the inversion-mode metal-insulator-semiconductor field-effect transistors.

Another object is to provide a method of making a heterojunction field-effect transistor having the capability for high frequency and microwave response due to the high transconductance and the prevention of minority carrier injection into the larger bandgap InP by the holes in the $Ga_{0.47}In_{0.53}As$ epilayer.

These and other objects of the invention will become more readily apparent from the ensuing description and claims when taken with the appended drawings.

BRIEF DESCRIPTION OF THE DRAWING

The drawing depicts a representative embodiment of a heterojunction inversion-mode metal-insulator-semiconductor field-effect transistor fabricated in accordance with the teachings of this inventive concept.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawing, a representative heterojunction source-drain insulated gate field-effect transistor 10 is depicted having a semi-insulating InP substrate 11 on which an epitaxial layer 12 of the p-type ternary alloy $Ga_{0.47}In_{0.53}As$ is grown. Its thickness may be of the order of several microns; however, the exact thickness is of no consequence since, instead an acceptor-doped p-type bulk $Ga_{0.47}In_{0.53}As$ might be used.

Photolithographic and etching techniques are used to make shallow troughs in the semi-insulating InP into which n^+ doped InP source and drain contacts 13 and 14 are deposited by a chemical vapor-phase transport reaction. This procedure makes symmetrical or asymmetrical n^+-p heterojunction contacts at the source and drain electrodes. It is to be noted that an essential feature in this regard is that the ternary alloy epilayer is, in fact, in contact with both the source and drain

contacts which are, optionally given a contact metalization layer 13*a* and 14*a* to enhance electrical coupling with other circuit components.

In order to prevent deposition of InP on the rest of the $Ga_{0.47}In_{0.53}As$, a silicon dioxide or silicon nitride coating 15 is deposited to a 1.0 micron thickness by a low temperature pyrolysis process. Specific windows 13*a'* and 14*a'* are opened in the dielectric coating to form specific windows for the deposition of the source and drain junctions 13 and 14. The windows are opened through the dielectric layer by any of several well known procedures, for example, one employing reactive sputtering or a similar technique.

Optionally, the heterojunctions between the source and drain contacts and the p-type ternary alloy epilayer can be made not only by the epitaxial growth by chemical vapor-phase techniques of n+InP as described above. Having the windows exposed to a stream of phosphine and hydrogen while the $Ga_{0.47}In_{0.53}As$ is heated to approximately 750° C. for about 15 minutes starts a chemical reaction. Since the vapor pressure of phosphorus is considerably greater (by about one order of magnitude) than that of arsenic, a chemical reaction takes place at the surface of the ternary alloy which produces a graded heterojunction in the source and drain contact windows. The composition of the heterojunction may vary from that of InP through the quaternary alloy $In_xGa_{1-x}As_yP_{1-y}$ up to the ternary alloy $Ga_{0.47}In_{0.53}As$. In either case the source and drain heterojunction are reverse biased with respect to the epitaxial layer or the bulk substrate and no current flows between them.

Gate dielectric layer 16, usually silicon dioxide in the order of 0.05 microns to 0.15 microns in thickness, is deposited upon the region between the source and drain contacts. Adequate care is required so that the surface of the $Ga_{0.47}In_{0.53}As$ is not perturbed. That is, its stoichiometry is preserved and its structure and morphology are not altered by the gate dielectric deposition process.

A metal electrode 17, usually aluminum, although other materials may be equally suitable, is used as the gate electrode and is superposed on the gate dielectric layer. The surface of the $Ga_{0.47}In_{0.53}As$ layer under the gate is normally slightly depleted. A positive potential applied to the gate electrode vis-a-vis the ternary alloy attracts electrons to the surface. In other words, the positive potential creates a surface inversion layer on the p-type $Ga_{0.47}In_{0.53}As$ which is isolated from the p-type bulk by an intermediate depletion region. The isolated surface layer produces a conductive channel between the source and drain n+ doped regions and the degree of depletion is a function of the potential applied to the gate. Thus, the gate potential modulates the conductance between the source and drain electrodes producing FET action.

The source and drain heterojunctions optionally are made of other materials which are lattice-matched to $Ga_{0.47}In_{0.53}As$ yet have a larger bandgap. A typical material is the ternary alloy $Al_{0.48}In_{0.52}As$ which has a large bandgap of 1.46 eV and is lattice-matched to InP as well as to $Ga_{0.47}In_{0.53}As$.

The reasons for using an inversion mode transistor based on the ternary alloy rather than some other material are described in detail in the above referenced pending patent application and intend to take full advantage of the specific high electron velocity of the $Ga_{0.47}In_{0.53}As$. Such a device might have power gain at frequencies much higher than presently available devices.

Specifically, the heterojunction source and drain contacts fabricated as described above will have a negligibly small current between the source and drain for large source-drain voltages of the order of 10 volts with a source-to-drain spacing of about four microns and for a gate voltage $V_y=0$. In addition, currents in the order of miliamps for V_y between one volt and ten volts are to be expected and the possibility of optical excitation of either heterojunction and optically-induced modulation of the heterojunction coupled with the transistor action of the I-MISFET also are realizable. High frequency and microwave response due to the high transconductance of the disclosed transistor and the prevention of the minority carrier injection into the larger bandgap InP by the holes in the $Ga_{0.47}In_{0.53}As$ are expected.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may be practiced otherwise than as specifically described.

What is claimed is:

1. A method of making an inversion mode metal-insulator-semiconductor field-effect transistor having heterojunction source and drain contact junctions comprising:

providing a semi-insulating InP semiconductor substrate;

growing a ternary alloy layer of p-type $Ga_{0.47}In_{0.53}As$ epitaxially on a portion of the semi-insulating InP semiconductor substrate;

coating the exposed semi-insulating semiconductor substrate and the ternary alloy layer with a dielectric;

opening source and drain contact windows through the dielectric coating and in contact with the ternary alloy layer;

exposing the open source and drain contact windows to a stream of phosphine and hydrogen while heating the p-type $Ga_{0.47}In_{0.53}As$ to about 750° C. for about 15 minutes to create a chemical reaction at the surface of the p-type $Ga_{0.47}In_{0.53}As$ producing a graded index heterojunction composed of InP through $In_xGa_{1-x}As_yP_{1-y}$ to $Ga_{0.47}In_{0.53}As$; and

superposing a metal gate electrode on the dielectric coated ternary alloy layer in a region lying between the heterojunction source and drain contacts.

2. A method according to claim 1 in which the steps of providing a semi-insulating InP semiconductor substrate and the growing of a ternary alloy layer are eliminated and in place of the layered structure an acceptor-doped p-type bulk $Ga_{0.47}In_{0.53}As$ is utilized.

3. A method according to claim 2 in which the step of opening includes a sputter etching of the dielectric layer.

* * * * *

END

FILMED

9-85

DTIC